EPXA1 Development Board

Rev 1.3

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Mechanical Parts

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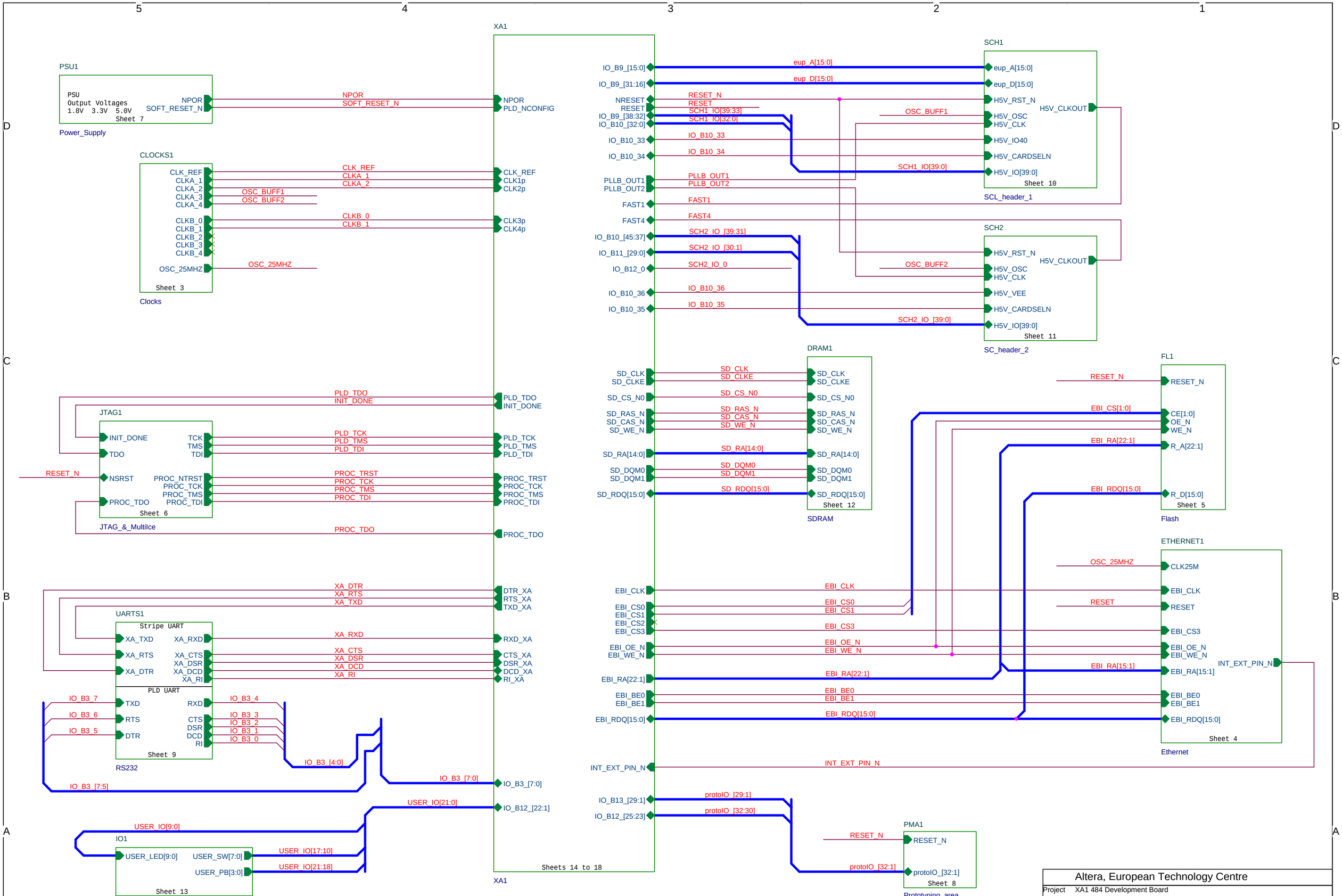

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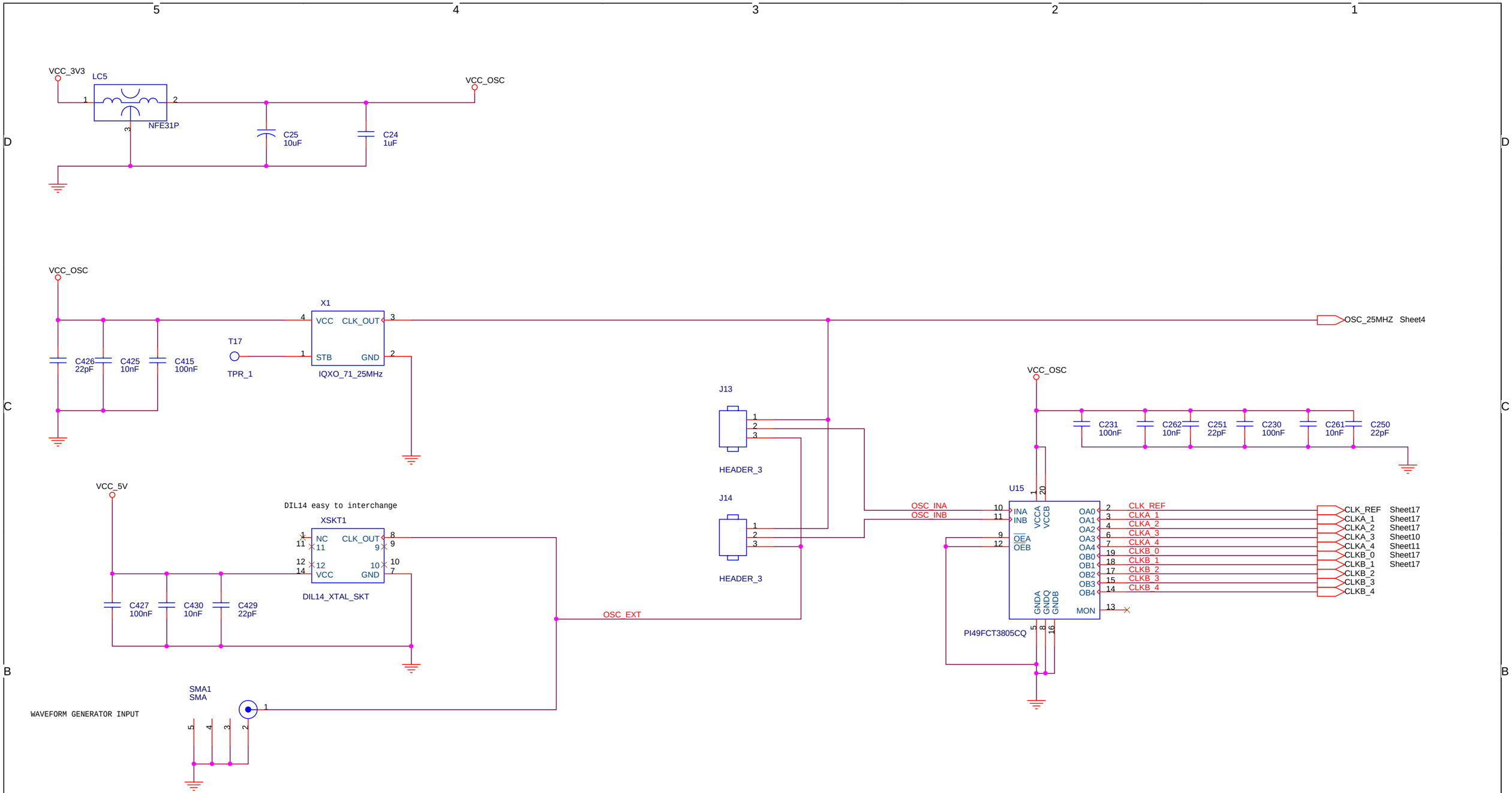

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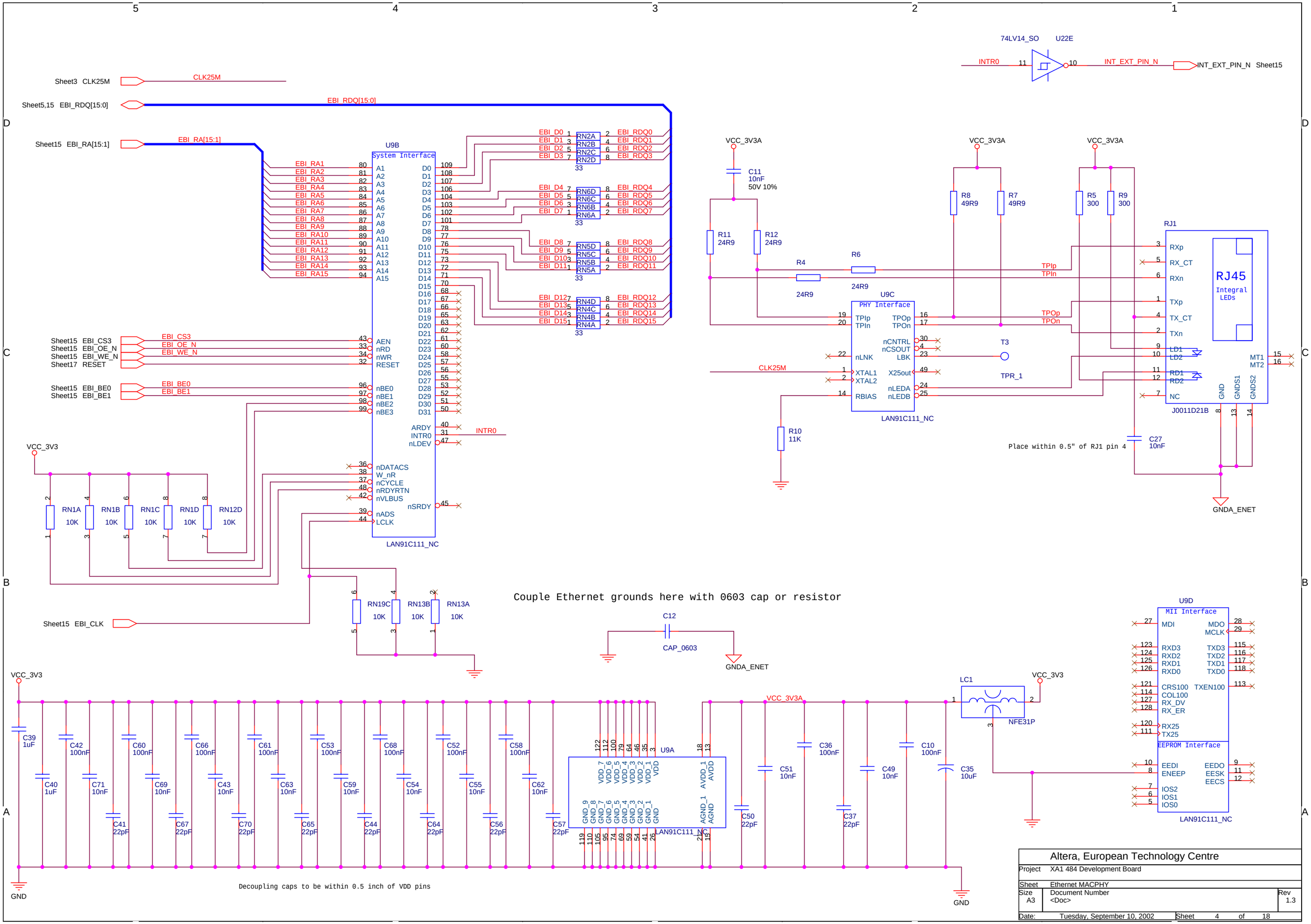

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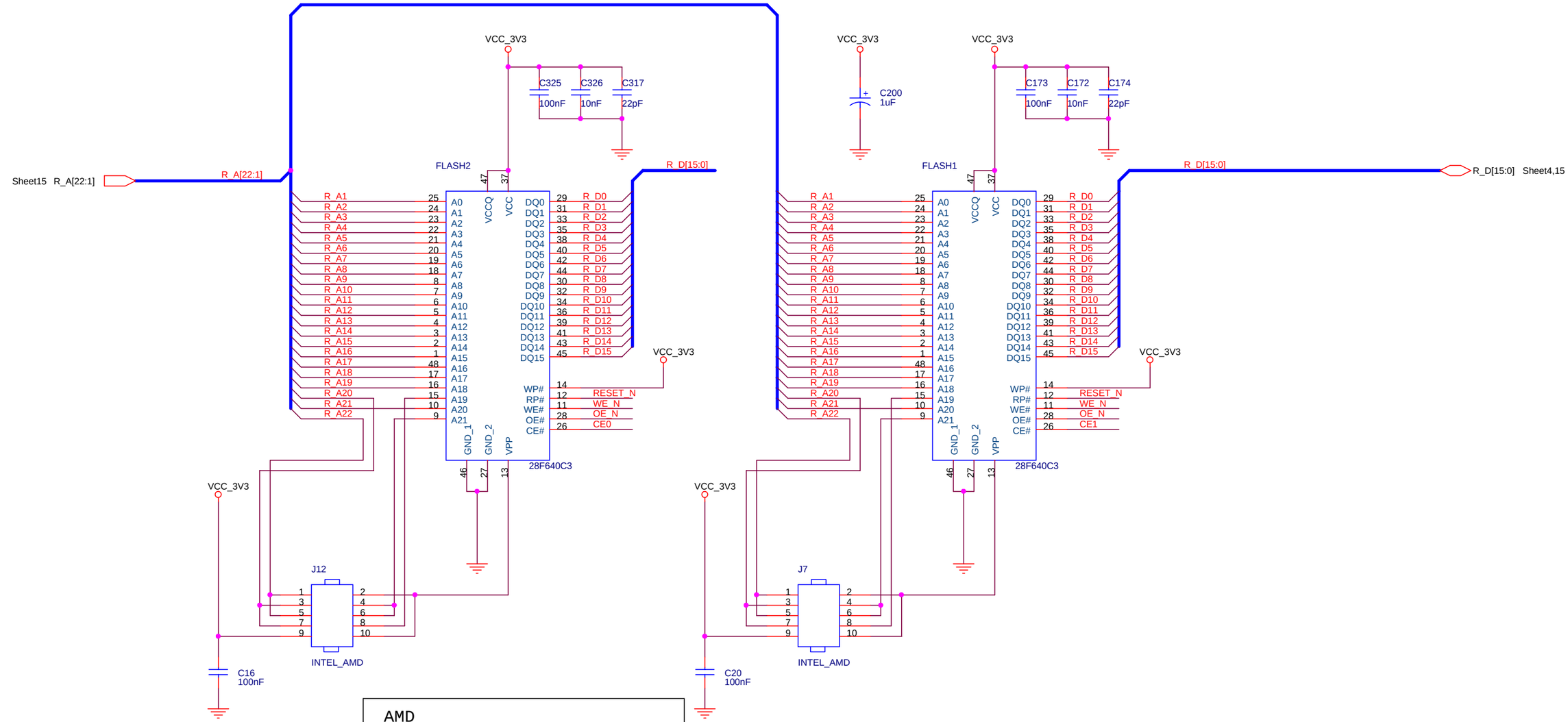

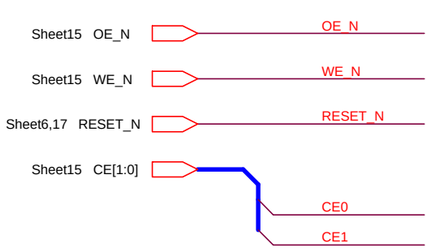


```
AMD
Connect 1 & 2, 3 & 4
1-------2
3-------4
5       6
7       8
9       10

INTEL
Connect 5 & 6, 7 & 8, 9 & 10
1       2
3       4
5-------6
7-------8
9-------10
```

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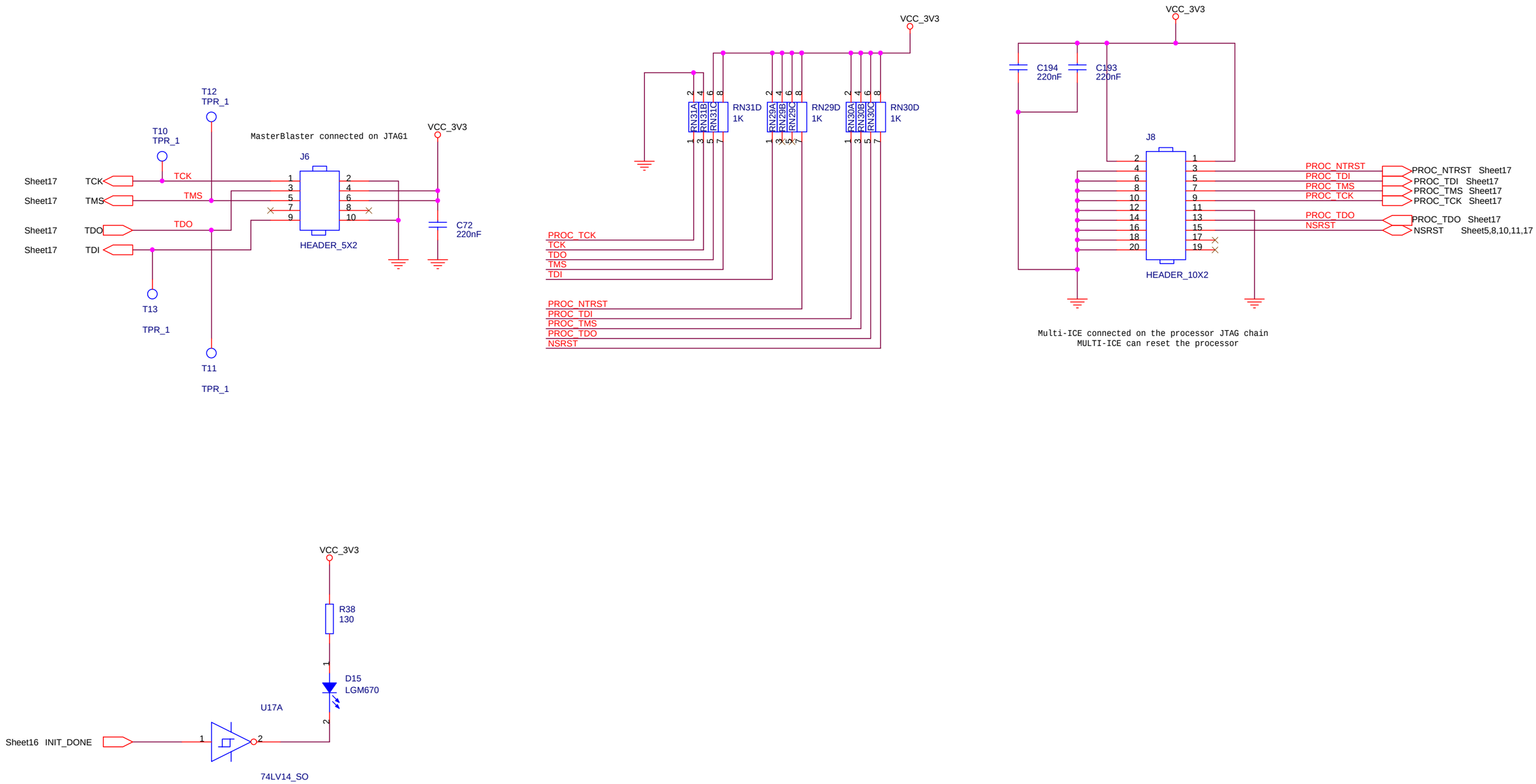

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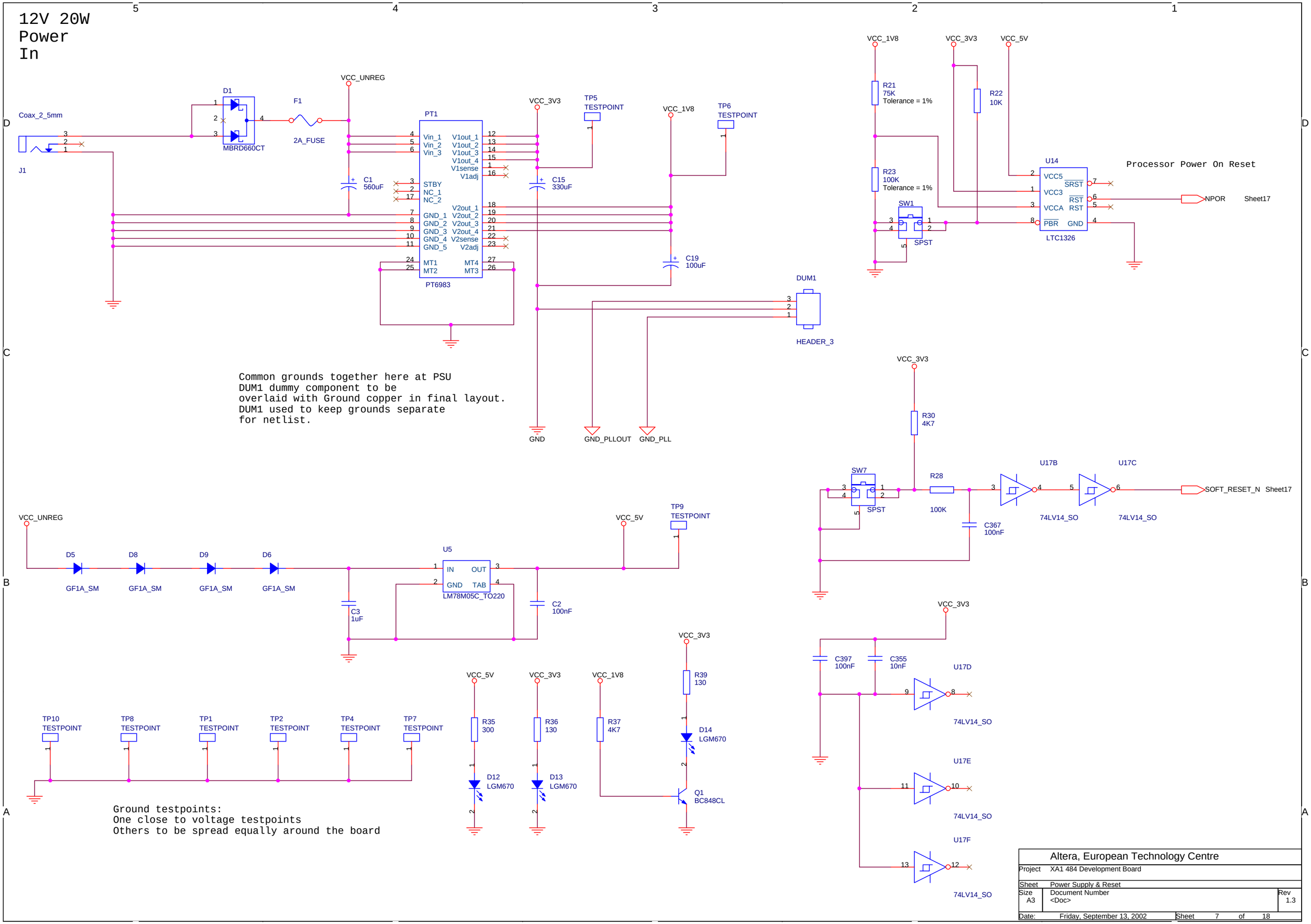
12V 20W Power In



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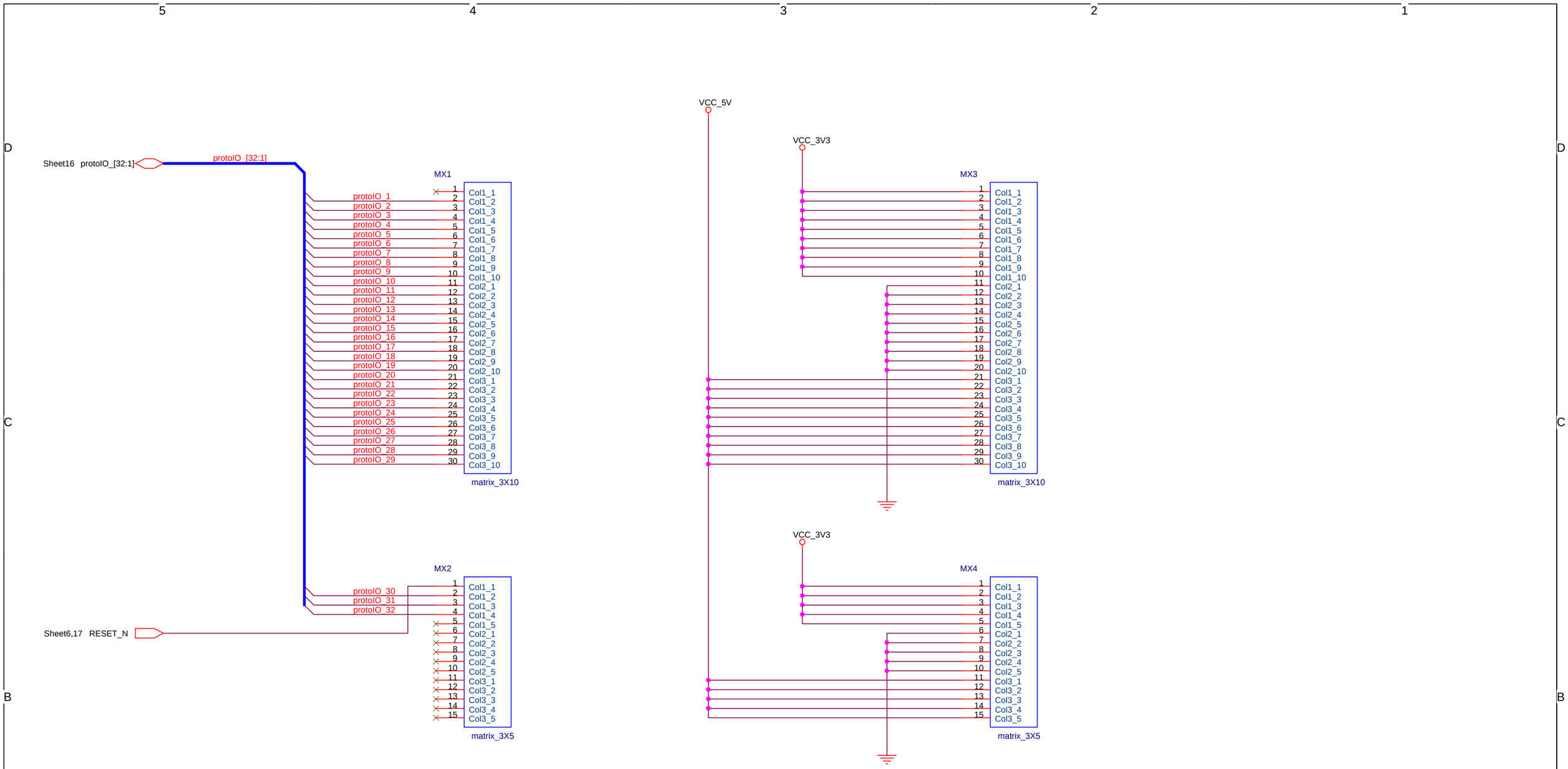

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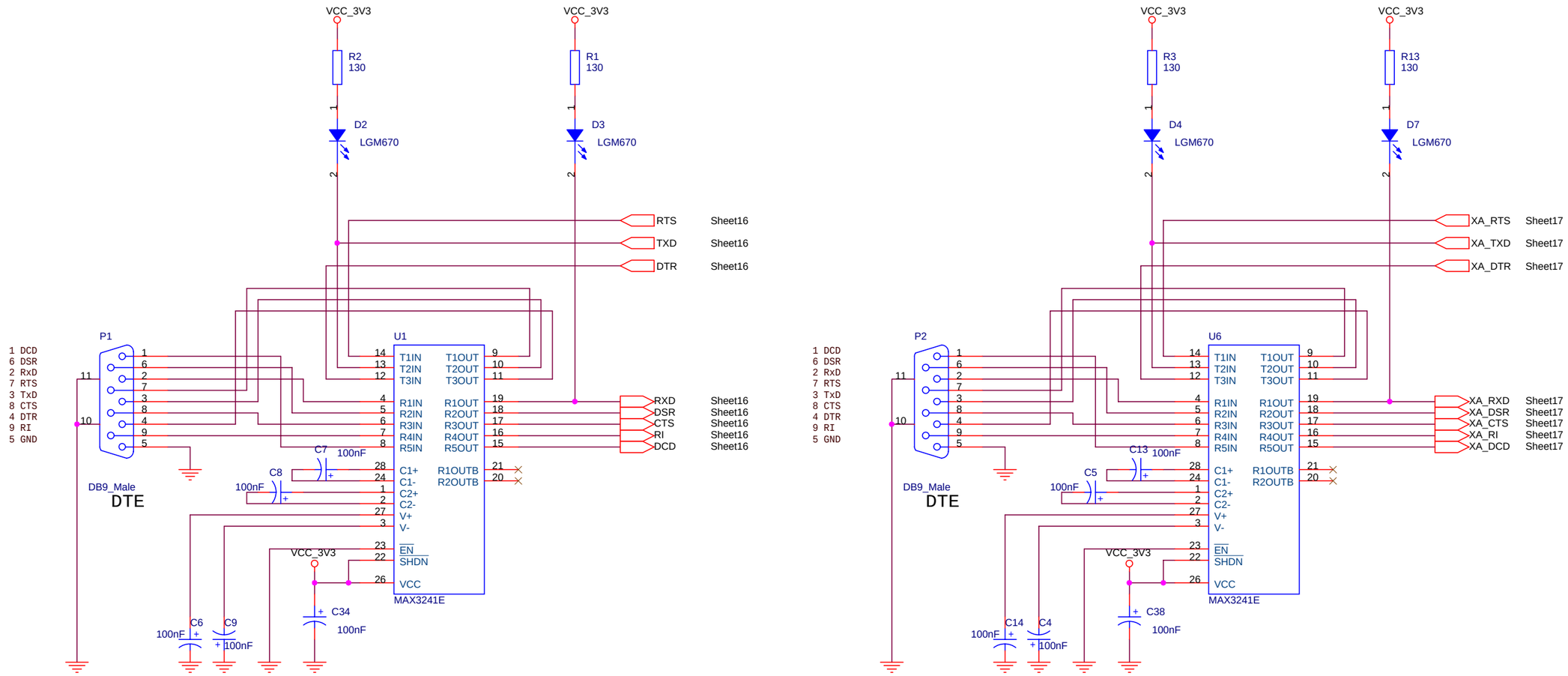

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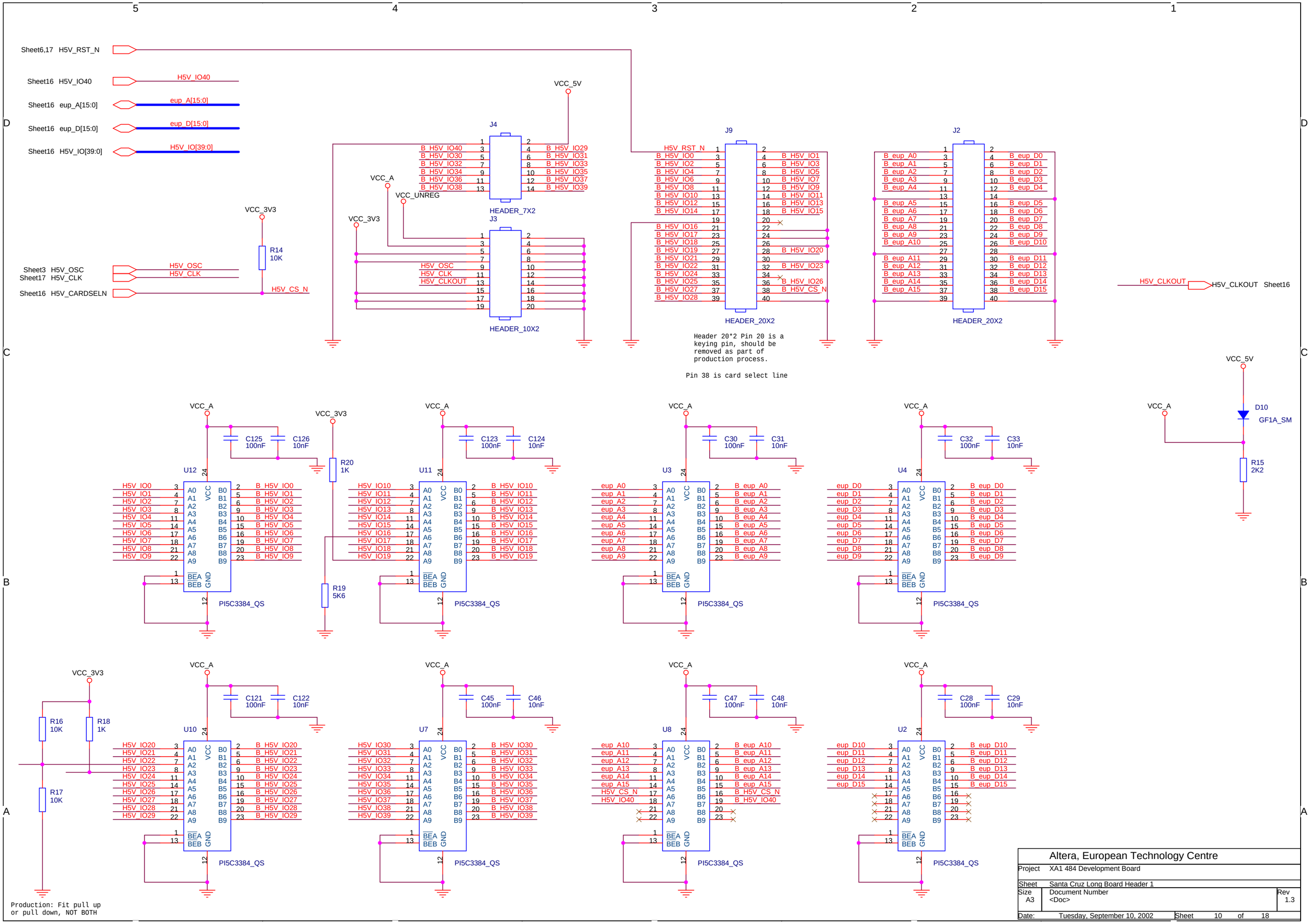

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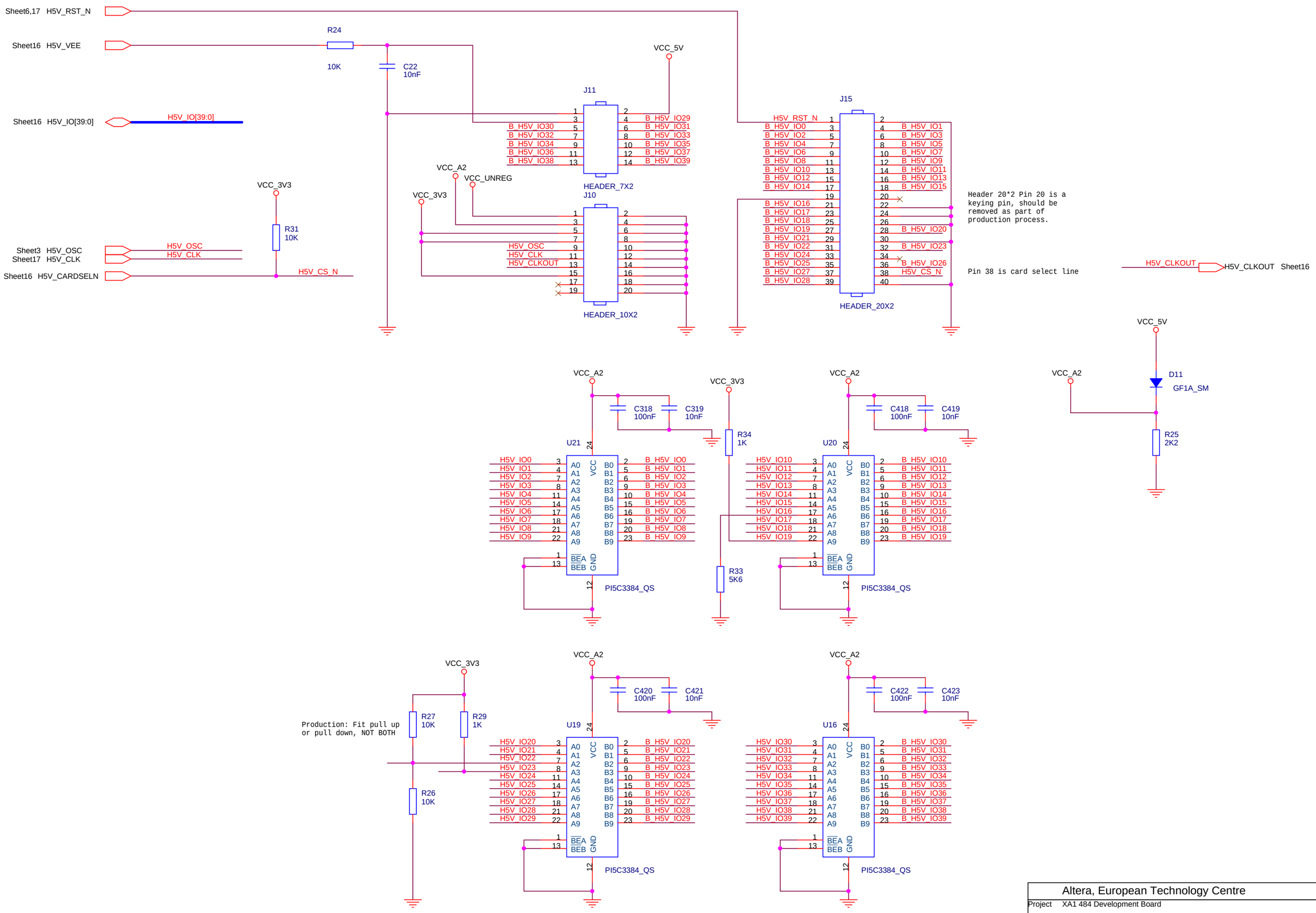

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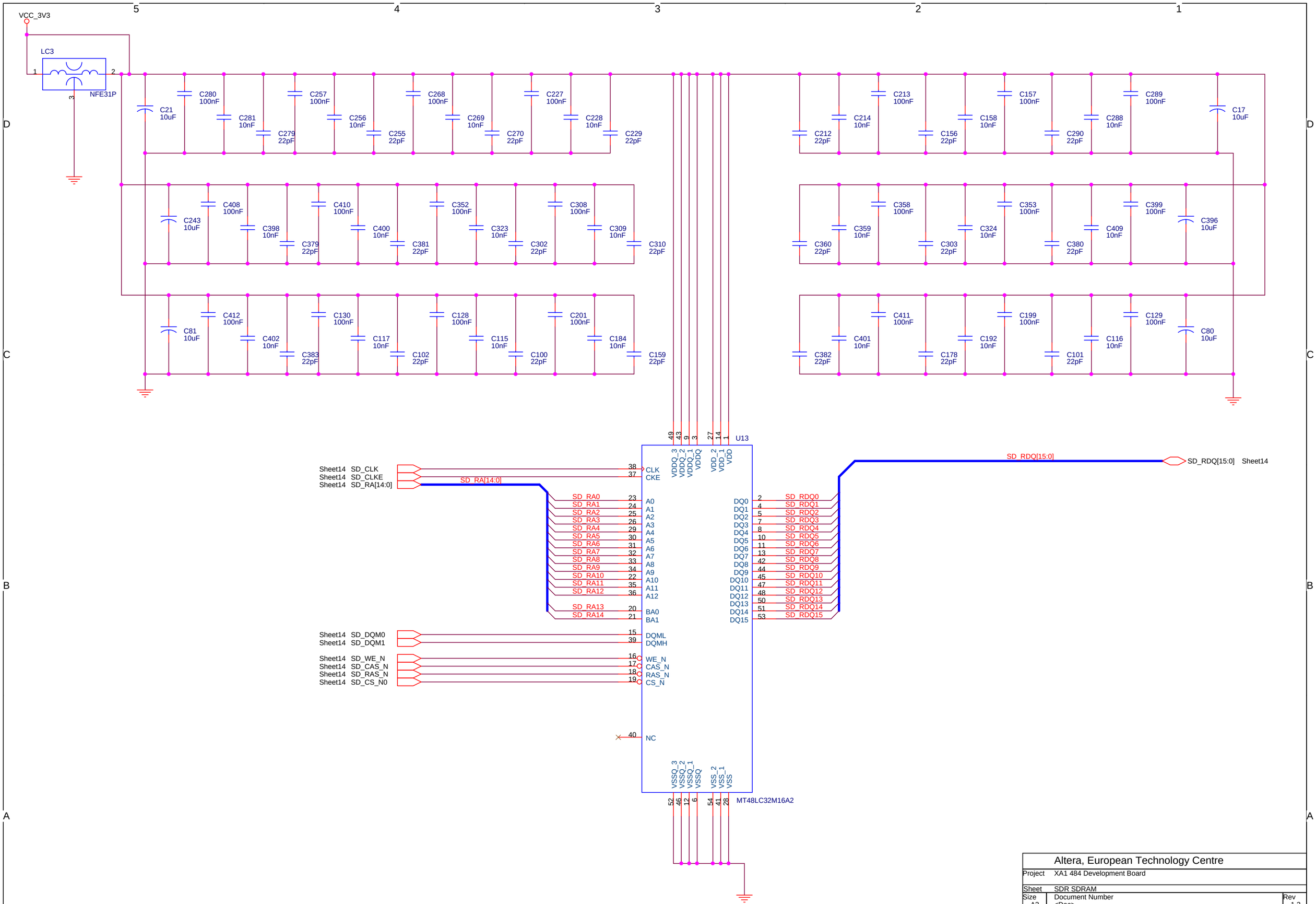

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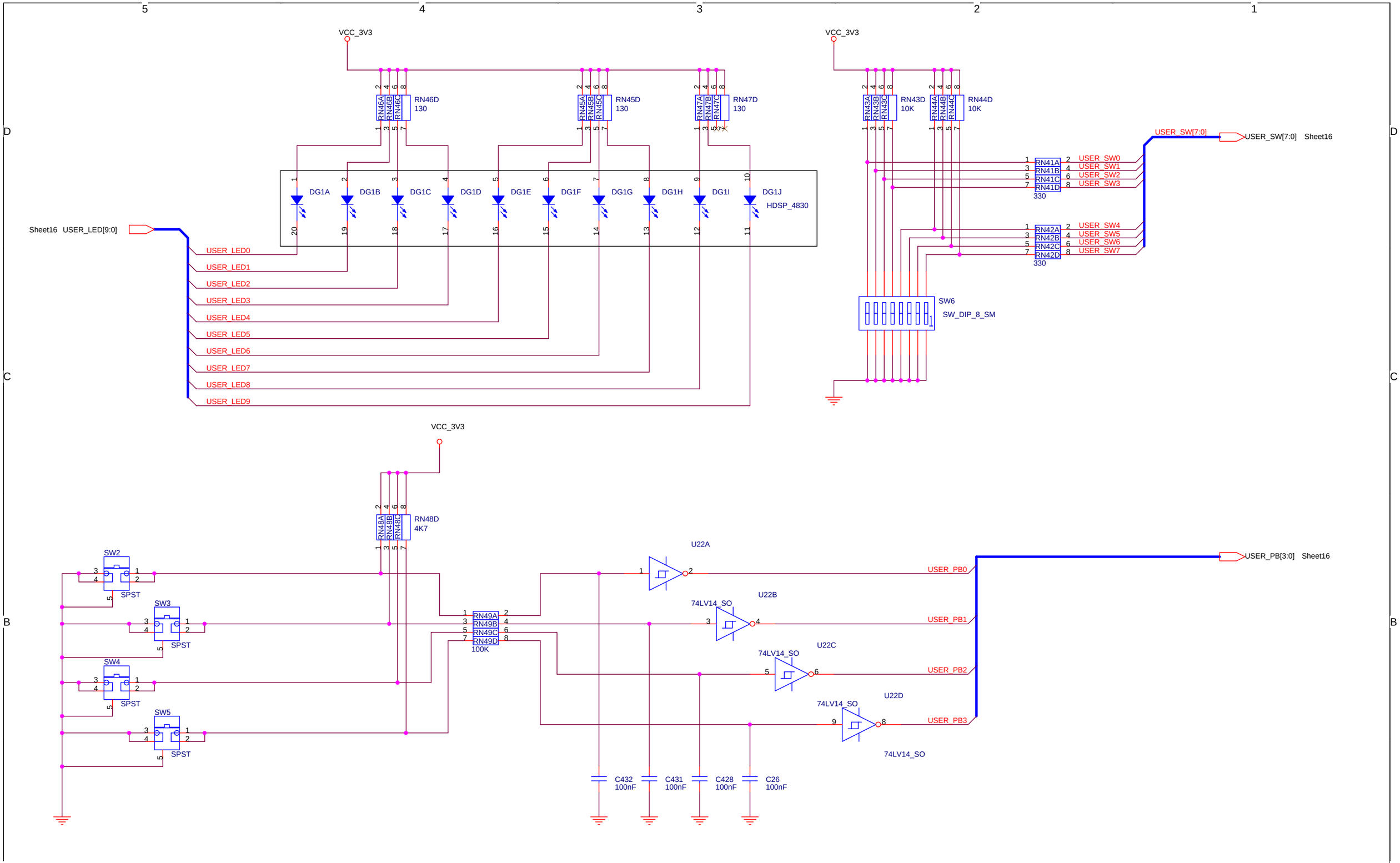

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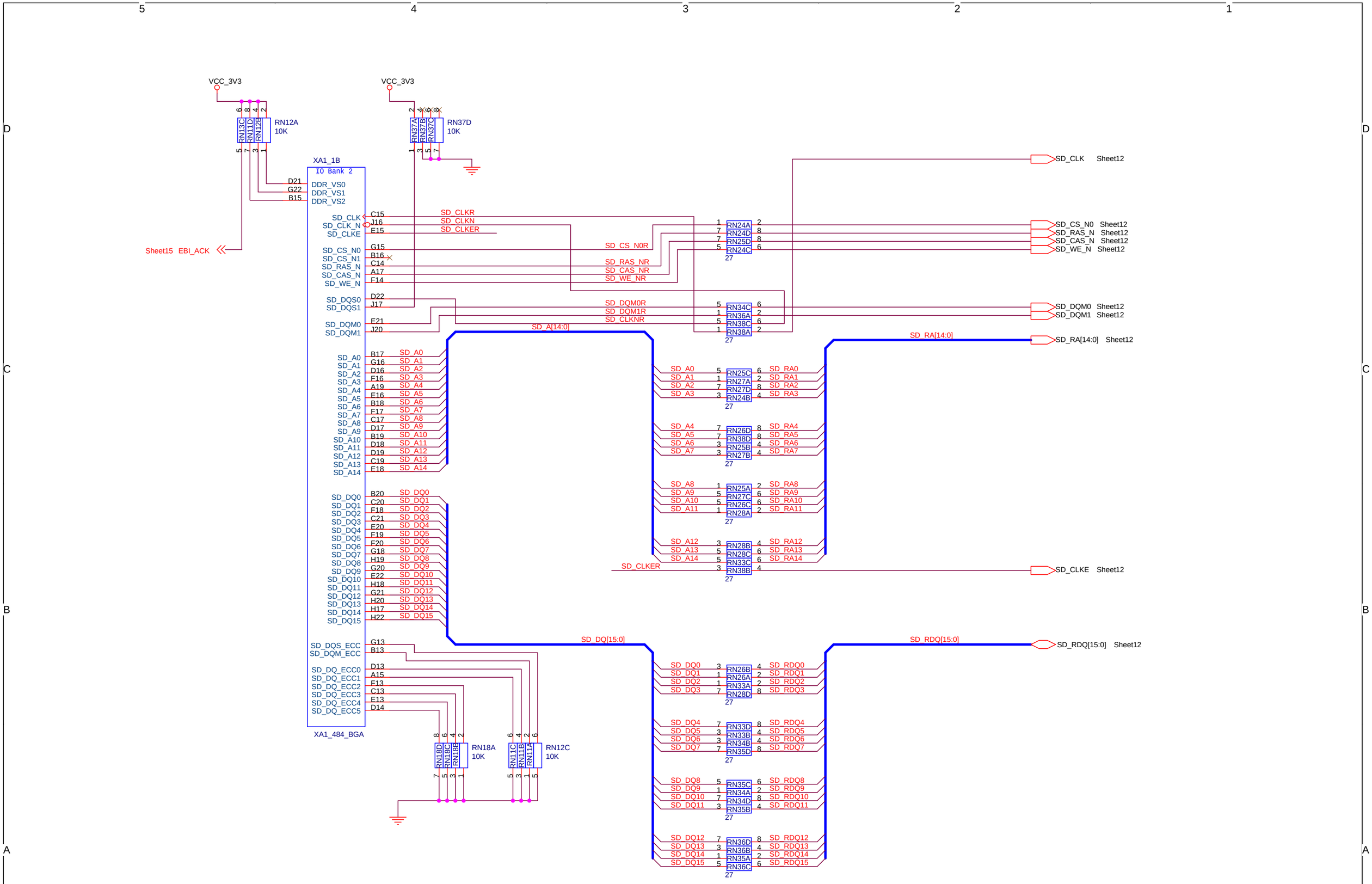

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Sheet	XA1 IO Bank 2 SDRAM Interface
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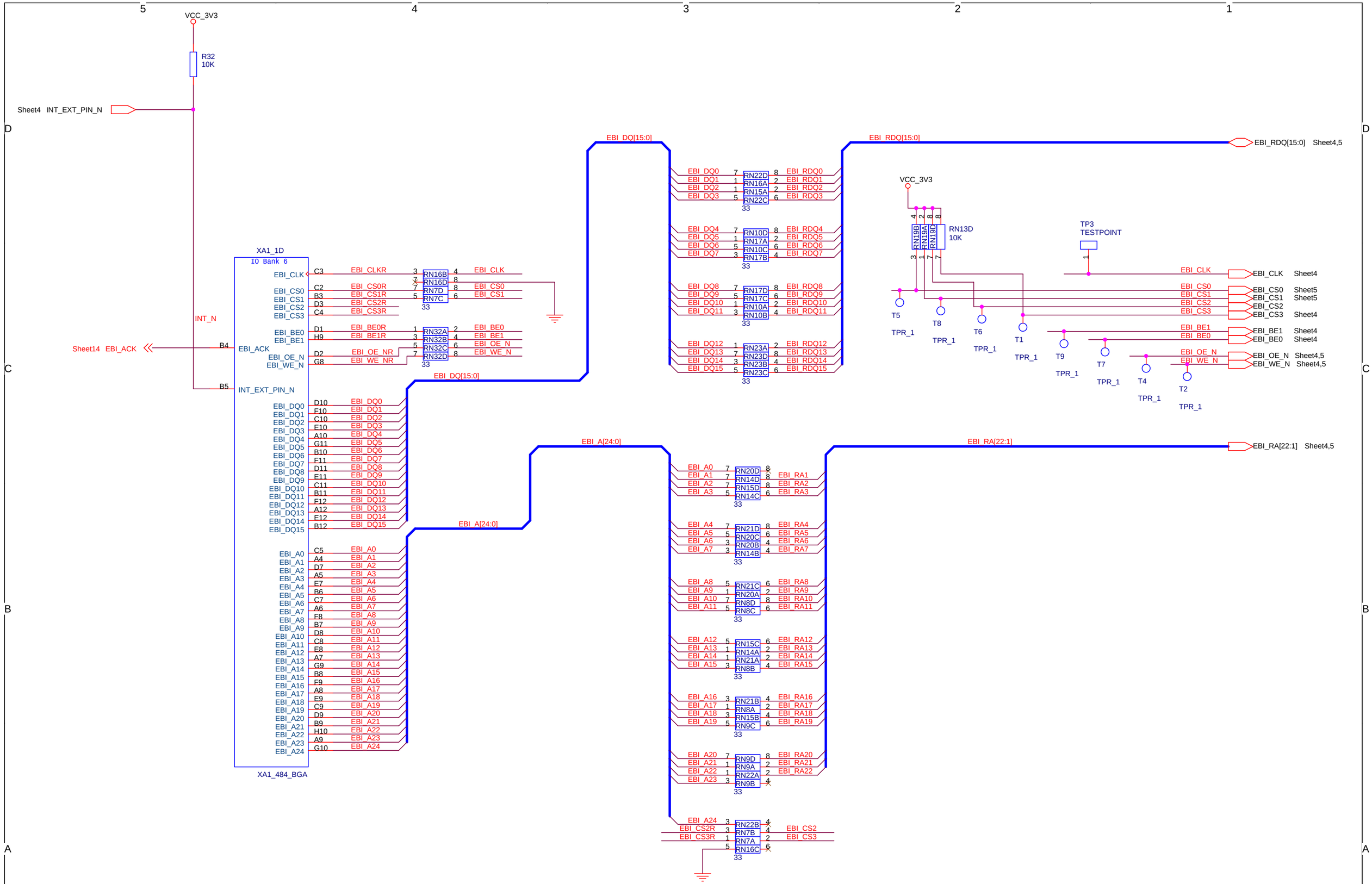

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Sheet	XA1 IO Bank 6 EBI
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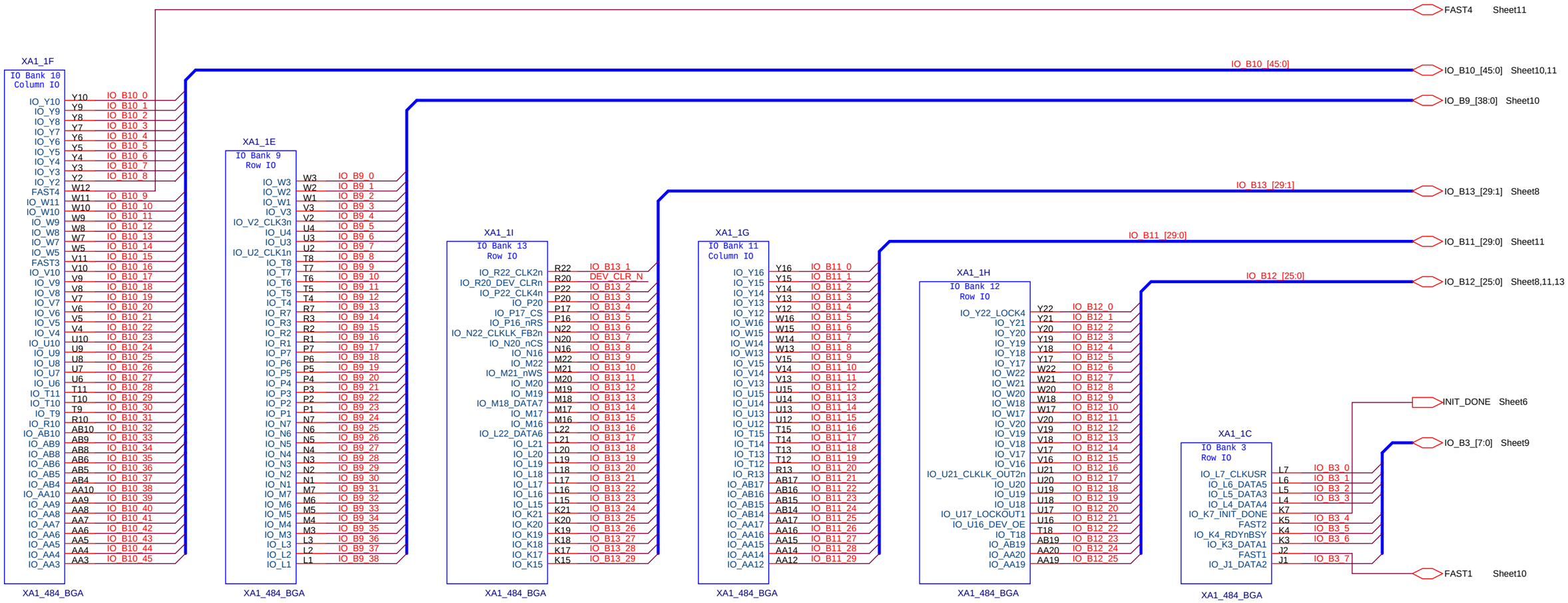

T16 & T17 placed together on PCB to allow use of PLD DEV_CLR signal.

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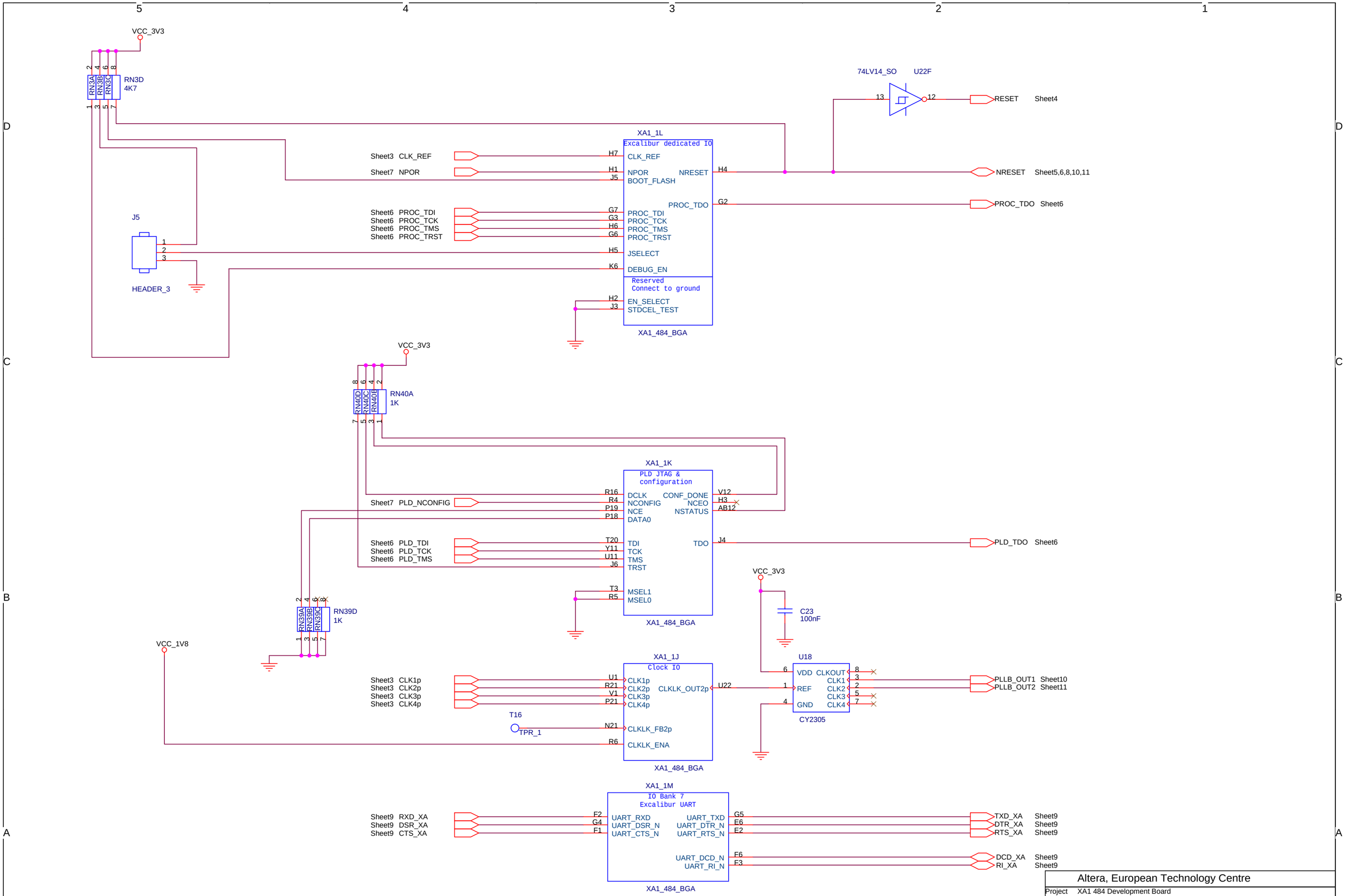

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Sheet	XA1 JTAG Configuration, UART, Clocks & Reset
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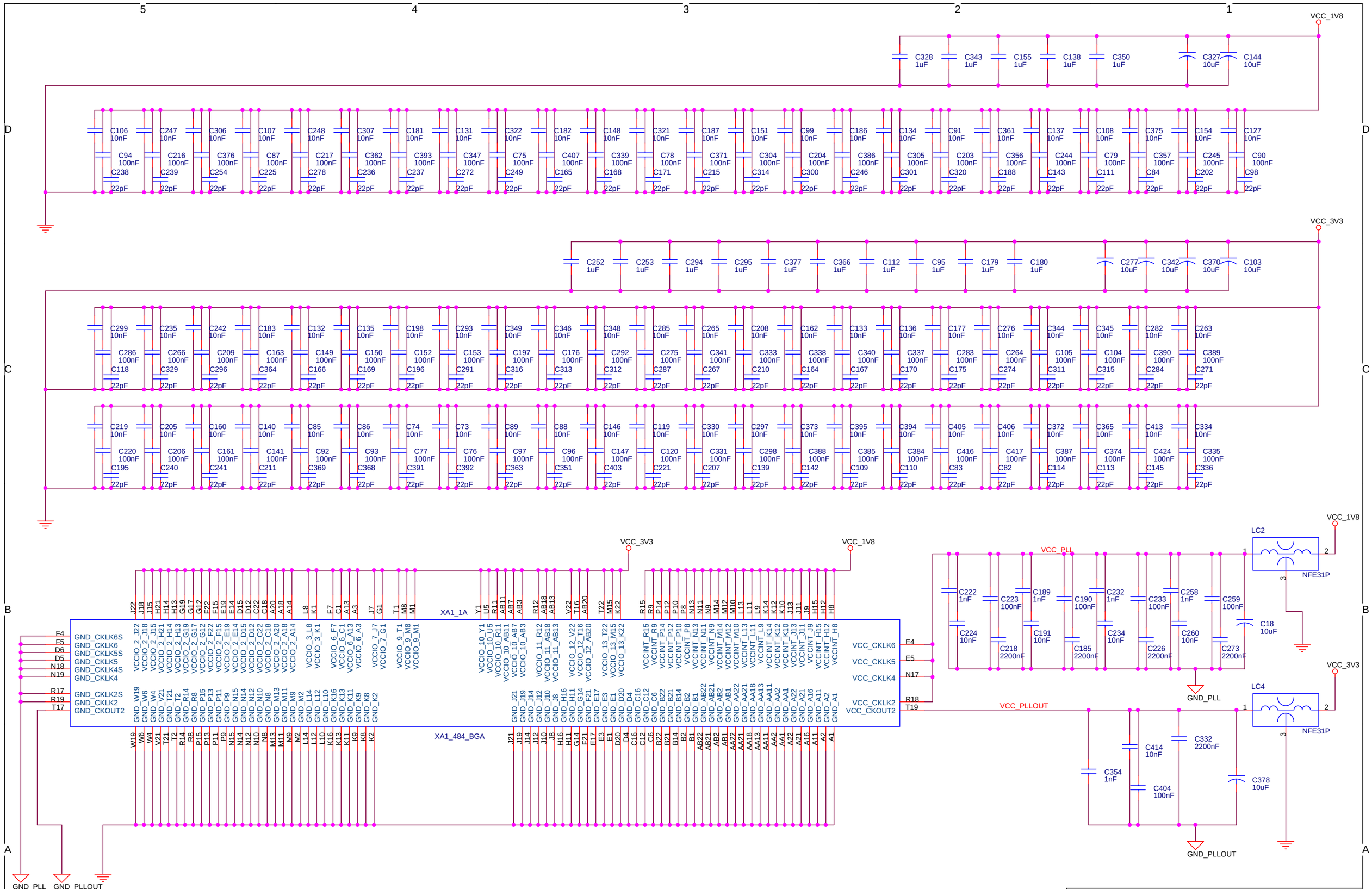

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1. XA1 Board PCB Layout Constraints and Information
Any deviations from these guidelines must be approved by the Altera design authority.
1.1 Component Placement
1.1.1 Overview
An example layout of the board is shown in figure 1.

The figure shall not be interpreted as a scale picture of the layout, rather as a sketch. The overall dimensions shall be in the range of 7" * 5.5". The position of the various functional blocks does not have to match this drawing and may be changed to meet routing constraints.
However, the board shall have an overall orientation as demonstrated in figure 1. This means cable connectors are at the back and the user I/O equipment faces the front side. The EPXA1 topmark shall be readable by the user in this position.
1.1.2 General
Board will be a single multilayer PCB in standard FR4. Cores and copper will use industry standard thicknesses and weights.
Capacitors and resistors may be placed on the top or bottom of the board. All other components should be placed on the top side of the board.
As far as is feasible all similar components should be placed with the same orientation on the board. i.e For ICs pin A1 or pin 1 at top left. Other components of similar type all vertical or horizontal for each type.
After layout is complete all components will be renumbered with ref 1 at the top left of the board, renumbering left to right, top to bottom.
All component and pin swaps to be documented and back annotated to the schematic.
The renumbering must be documented and back annotated to the schematic.
A DRC check and a Valor manufacturing check will be run on the completed PCB layout.
The documentation files for component and pin swaps, documentation files for component renumbering and the result files from DRC and Valor will be sent to the Altera design authority for review and will form part of the deliverables.
1.1.3 Decoupling capacitors
Decoupling capacitors for this board come in a range of values and packages:
The 0603 package supports all values as follows:
50V up to 10nF
16V up to 100nF
10V up to 1uF
The 1206 package supports higher values up to 2.2uF.
The 10uF caps will have to be tantalum, size is dependent on voltage.

All caps will be placed with the lower value caps nearest the pins being decoupled and values working higher as they move further from the pins.

The 0603, 1nF to 100nF caps shall be placed as close to the power pins of the device being decoupled as possible, Maximum within 0.5".

The 1206, 1uF to 2.2uF caps are designed to provide decoupling for multiple pins and smaller caps and may be placed within 2" of the pins being decoupled.

The larger values are generally used as bulk decoupling and should be placed within 0.5" of the regulator/power module outputs.

1.1.4 Resistor Packs
The design makes use of chip resistor arrays Bourns CAY16 series. Each array contains 4 isolated 0603 resistors in a 1206 size package.
The specific resistor used within any particular set of common value arrays may be swapped to make routing easier. These component/pin swaps must be documented and back annotated to the schematic.

1.1.5 XA1 IO
The generic PLD IO used in sheet "XA1_IO_banks_3_9_10_11_12_13" may be pin swapped but only after consultation with the Altera design authority.
These pin swaps must be documented and back annotated to the schematic.

Exceptions to this, which may not be swapped, are the pins:
XA1_1C ,J2 ,FAST1
XA1_1C ,K7,INIT_DONE
XA1_1F ,W12 ,FAST4

1.2 Track Routing Constraints
1.2.1 General
Track and gap sizes shall be as large as possible given the constraints of routing out from under the FPGA.
7 thou track 8 thou gap would be the prefered minimum. Suggested routing in Altera Device Package Data Book 1999 should be followed.
No signals should cross power or ground planes other than the ones they are referenced to. No signals should cross gaps in planes without agreement from the Altera design authority.
Signal tracks should be impedance controlled at 50 ohms.
1.2.2 Power and ground Planes
Complete unbroken power and ground planes will be provided for the 3.3V (VCC_3V3) and 1.8V (VCC_1V8) supplies both reference digital ground, GND.
Other supplies which need to be routed from the main PSU are :
VCC_UNREG
This needs to be kept well away from all signal lines and other supply voltages but may use digital ground.

5V VCC_5V
May be routed as power and ground islands on either signal layers or dedicated split plane power and ground layers. Could be routed at edge of another power plane. May use digital ground.

VCC_OSC
Derived from 3.3V.
These may be routed as power and ground islands on either signal layers or dedicated split plane power and ground layers. May use digital ground.

PLL 1.8V VCC_PLL, GND_PLL
PLL 3.3V VCC_PLLOUT, GND_PLLOUT
These may be routed as power and ground islands on either signal layers or dedicated split plane power and ground layers. Each of these needs it's own dedicated ground.

Nios header busswitch supplies 4V derived from 5V through diodes.
VCC_A
VCC_A2
These should be derived from the 5V supply tracks feeding the Nios headers and can be tracked locally to the busswitch devices. An independent ground is not required and they can be referenced to digital ground.

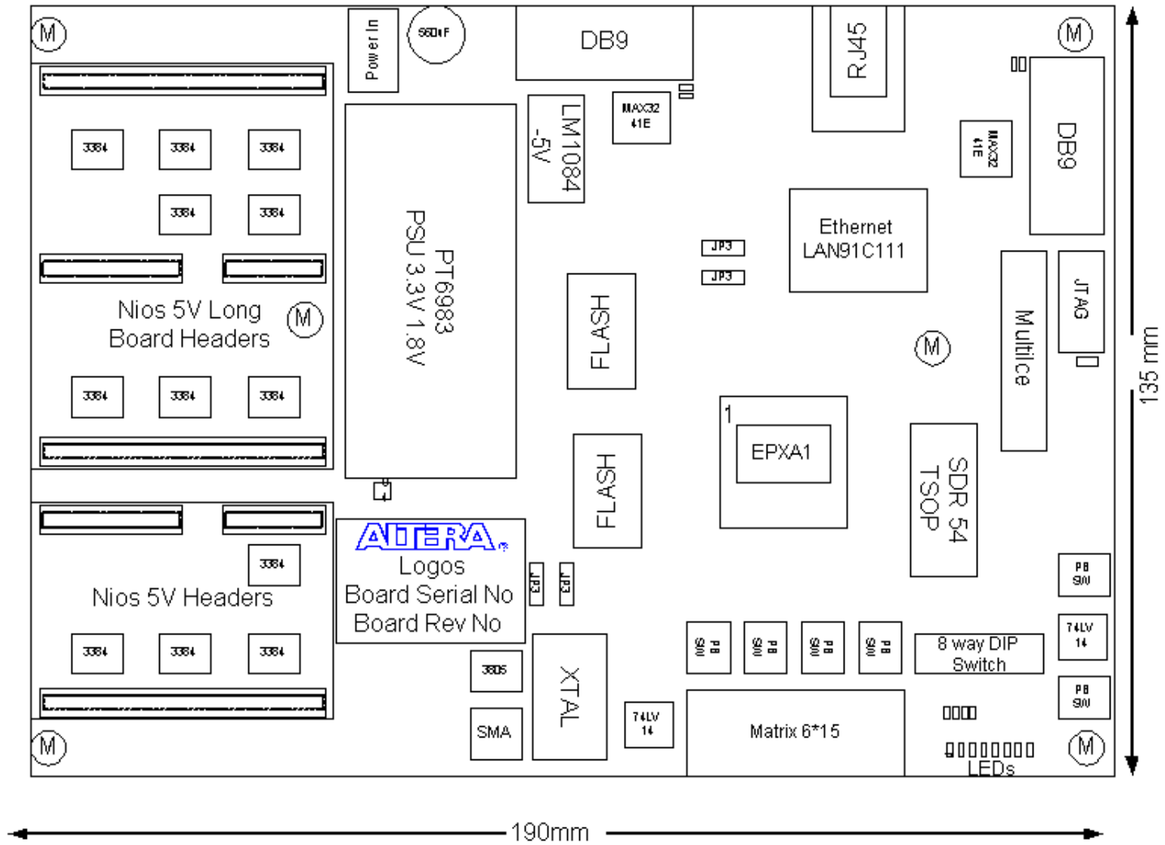
VCC3V3A, GNDA_ENET
This is the Ethernet analog power and ground ground. It should be an island surrounding the Ethernet RJ45 connector and associated analog pins on the LAN91C111 MACPHY. It has a single 0805 connection to GND.
1.2.3 Clocks
The following tracks must be treated as clock signals:
OSC_25MHZ
OSC_EXT
OSC_INA, OSC_INB, OSC_BUFF1, OSC_BUFF2
CLK_REF
CLK_A1, CLK_A2, CLK_A3, CLK_A4
CLK_B0, CLK_B1, CLK_B2, CLK_B3, CLK_B4
CLK1p, CLK2p, CLK3p, CLK4p, CLKLK_OUT2p
H5V_CLK, H5V_OSC, H5V_CLKOUT
SD_CLK
PLD_TCK, PROC_TCK, TCK

1.2.4 SDR SDRAM Interface
The SDRAM interface bus is all the signals prefixed SD_ These interface to just one SDR SDRAM device.
Overall routed length should be kept at less than 3".
Track lengths for all signals shall be matched to within 2%. This includes both overall signal length through series resistors and individual track segment lengths.
Tracks must be impedance controlled at 50 ohms.

1.2.5 EBI Interface : FLASH & Ethernet LAN91C111
The EBI interface bus is all the signals prefixed EBI_ These may be daisy chained to the 2 flash devices and the Lan chip.
Overall routed length should be kept as short as possible and in any case no longer than 6".
Track lengths for all signals shall be matched to within 5%. This includes both overall signal length through series resistors and individual track segment lengths.
Tracks must be impedance controlled at 50 ohms.
1.2.6 JTAG Interfaces
There are 2 JTAG interfaces for the PLD and the Processor (PROC).
Overall routed length should be kept as short as possible and in any case no longer than 6". The JTAG interface signals for each interface should have track lengths for all signals matched to within 15%. This includes both overall signal length through series resistors and individual track segment lengths.
Tracks must be impedance controlled at 50 ohms.

JTAG PLD signals are:
TMS
TCK
TDI
TDO
NSRST

JTAG PROC signals are:
PROC_TMS
PROC_NTRST
PROC_TCK
PROC_TDI
PROC_TDO
1.3 Silkscreen
The silkscreen must include the board name "EPXA1 Development Board" and the PCB revision number "Rev 0.0"
The silkscreen must include a blank white square for handwriting the Board rel number and serial number on.
The silkscreen must include row and column numbers/letters for the matrix area.



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