



It would be good to put a pad for a resistor here if gain is needed. 4/13/99 gtp

R54 needs to be rise 2010 or 2512 (1W). 4/13/99 gtp

The DS1040 pull-down output may be faster than the pull-up, but the input logic threshold of the 3.3V FPGA input may give more prompt detection of change of state.

The propagation delay of the DS1040 is ~5ns. ORing the output of the DS1040 with the output of the comparator inside the FPGA may result less over all propagation delay. On the other hand, if the trace from the comparator to the FPGA is long, the additional capacitance may adversely affect the detection of trigger pulses by the One-shot.

The binary coded Width pins of the DS1040 for both the OneSPE and MultiSPE One-Shots are paralleled to save FPGA pins as it is likely they would both be set to the same delay. Suitable parts are the -B50, -D60, -D70, -75, and -100 are probably versions of the DS1040 which look promising for this project.

As of Jan 20, 1999, the output of the unamplified channel ATWD channel is 2.0V for a 200 SPE signal. The amplified channel of the ATWD, therefore, saturates at about 12.5 SPE. The PMT signal is about 10 mV per SPE.

The shaped signal path design was from Harold Yaver of the Engineering Department. -Modifications added to insure stable offset behavior, and to offset the output to match the input range of the ADC

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